B7 Cncl'd

19. (Amended) The method of manufacturing semiconductor devices according to claim 9 further comprising a step wherein, prior to securing said semiconductor chip to said securing area, testing of said semiconductor chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.

Please add the following new claim:

B8

20. (New) A semiconductor device, comprising:

a plurality of bond pads arranged on a semiconductor chip, each of said bond pads in said plurality comprising a bond region and a probe region, said plurality of bond pads comprising two groups of bond pads, a first group of bond pads arranged with bond regions in a first direction and probe regions in a second direction, and a second group of bond pads arranged with probe regions in said first direction and bond regions in said second direction, wherein said first and second groups are arranged in an alternating manner with each member of said first group adjacent a member of said second group.

REMARKS

Reconsideration of the above-referenced application in view of the amendments and the following remarks is respectfully requested.

Claims 1-19 were pending in this case. New Claim 20 has been added. Claims 1, 2, 3, 7, 8, 10, 18, and 19 have been amended to more clearly define the scope of the claimed invention.

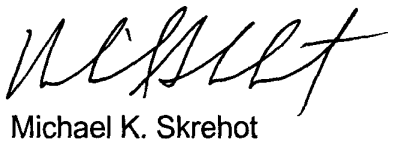
Claims 1-6 and 11-17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Bell (U.S. Patent No. 6,373,143) in view of Hikita, et al. (U.S. Patent No. 6,369,407) and further in view of Wensel, et al. (U.S. Patent No. 6,291,899). Claim 1, as amended, includes a plurality of bonding pads "wherein said plurality of bonding pads comprises a first group of bonding pads with said first regions in a first direction and said second regions in a second direction, and a second group of bonding pads provided with said second regions in said first direction and said first regions in said second direction." Neither the Bell, Hikita, nor Wensel reference teaches or suggests such a feature. Thus, the combination of those references fails to teach or suggest all of the features of the claimed invention. Applicant therefore respectfully submits that Claim 1 is patentable over the references of record. Claims 2-6 and 11-17 depend from Claim 1 and are therefore patentable over the references of record for at least the reasons presented above.

Claims 7-10, 18, and 19 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Bell (U.S. Patent No. 6,249,675) in view of Hikita, et al. (6,369,407) and further in view of Wensel, et al. (6,291,899). Claim 7, as amended, includes the feature of "wherein said plurality of bonding pads comprises a first group of bonding pads with said first regions in a first direction and said second regions in a second direction, and a second group of bonding pads provided with said second regions in said first direction and said first regions in said second direction." Neither the Bell, Hikita, nor Wensel reference teaches or suggests such a feature. Thus, the combination of those references fails to teach or suggest all of the features of the claimed invention. Applicant therefore respectfully submits that Claim 7 is patentable over the references of record. Claims 8-10, 18, and 19 depend from Claim 7 and are therefore patentable over the references of record for at least the reasons presented above.

New Claim 20 includes the feature of "a plurality of bond pads arranged on a semiconductor chip, each of said bond pads in said plurality comprising a bond region and a probe region, said plurality of bond pads comprising two groups of bond pads, a first group of bond pads arranged with bond regions in a first direction and probe regions in a second direction, and a second group of bond pads arranged with probe regions in said first direction and bond regions in said second direction, wherein said first and second groups are arranged in an alternating manner with each member of said first group adjacent a member of said second group." Neither Bell reference, nor the Hikita or Wensel references teach or suggest such an alternating pad arrangement. Therefore, Applicant respectfully submits that Claim 20 is patentable over the references of record.

Applicant respectfully requests reconsideration and withdrawal of the rejections and allowance of Claims 1-20. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,



Texas Instruments Incorporated
P.O. Box 655474, M/S 3999
Dallas, TX 75265
Phone: 972 917-5653
Fax: 972 917-4418

Michael K. Skrehot
Reg. No. 36,682

Version with Markings to Show Changes Made

In the Claims:

1. (Twice Amended) A semiconductor device comprising:

a semiconductor chip upon which are disposed roughly upon a straight line a plurality of bonding pads, each of said bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction substantially perpendicular to said straight line, wherein said plurality of bonding pads comprises a first group of bonding pads with said first regions in a first direction and said second regions in a second direction, and a second group of bonding pads provided with said second regions in said first direction and said first regions in said second direction,

a member provided with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals and a securing area for securing said semiconductor chip,

a plurality of conductor wires that electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors, and

an encapsulating member that encapsulates said semiconductor chip and said plurality of conductor wires.

2. (Amended) The semiconductor device according to claim 1 wherein said first and second groups of bonding pads are alternately arranged [plurality of bonding pads comprise first bonding pads provided with said first regions toward the edge of said semiconductor chip and second bonding pads provided with said second regions toward the edge of said semiconductor chip, and said first and second bonding pads are disposed alternately roughly upon a straight line].

3. (Twice Amended) The semiconductor device according to claim 1 wherein said plurality of bonding pads are rectangular in shape with their [with their] short sides lying in a direction along the edges of said semiconductor chip.

7. (Twice Amended) A method of manufacturing semiconductor devices comprising:

disposing roughly upon a straight line on a semiconductor chip a plurality of bonding pads containing a first region as a connection region and a second region for making contact with a testing probe, and said first and second regions are lined up in a direction perpendicular to said straight line, wherein said plurality of bonding pads comprises a first group of bonding pads with said first regions in a first direction and said second regions in a second direction, and a second group of bonding pads provided with said second regions in said first direction and said first regions in said second direction,

providing [and] a member [provided] with a plurality of conductors containing a third region as a connection region electrically connected to each of a plurality of external connection terminals, and a securing area for securing said semiconductor chip [are secured], and

disposing a plurality of conductor wires to electrically connect said first regions of said plurality of bonding pads to said third regions of said plurality of conductors.

8. (Amended) The method of manufacturing semiconductor devices according to claim 7 wherein said first and second groups of bonding pads are alternately arranged [plurality of bonding pads comprise first bonding pads provided with said first regions toward the edge of said semiconductor chip and second bonding pads provided with said second regions toward the edge of said semiconductor chip, and said first and second bonding pads are disposed alternately roughly upon a straight line].

10. (Twice Amended) The method of manufacturing semiconductor devices according to claim 7 further comprising a step wherein, prior to [said] securing said semiconductor chip to said securing area [step], testing of said semiconductor chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.

18. (Amended) The method of manufacturing semiconductor devices according to claim 8 further comprising a step wherein, prior to [said] securing said semiconductor chip to said securing area [step], testing of said semiconductor chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.

19. (Amended) The method of manufacturing semiconductor devices according to claim 9 further comprising a step wherein, prior to [said] securing said semiconductor chip to said securing area [step], testing of said semiconductor chip is performed by putting test probes into contact with the second regions of said plurality of bonding pads.

Please add the following new claim:

20. (New) A semiconductor device, comprising:

a plurality of bond pads arranged on a semiconductor chip, each of said bond pads in said plurality comprising a bond region and a probe region, said plurality of bond pads comprising two groups of bond pads, a first group of bond pads arranged with bond regions in a first direction and probe regions in a second direction, and a second group of bond pads arranged with probe regions in said first direction and bond regions in said second direction, wherein said first and second groups are arranged in an alternating manner with each member of said first group adjacent a member of said second group.